New Claims

44. A method of forming a floating gate transistor comprising:

forming a first layer of polysilicon to a first thickness on a gate dielectric disposed on a substrate;

doping the first layer to a degree sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.;

after the doping, forming a second layer of polysilicon over the first layer of polysilicon to a second thickness;

oxidizing the substrate to form a first oxide layer over the second layer of polysilicon;

forming a layer of nitride over the first oxide layer;

oxidizing the substrate to form a second oxide layer over the layer of nitride;

forming a third layer of polysilicon over the second oxide layer; and

etching at least some of the layers to provide a floating gate transistor over the substrate.

45. The method of claim 44, wherein the first and second thicknesses are substantially the same.

46. The method of claim 44, wherein the first and second thicknesses are different.

D3 cont.

47. The method of claim 44, wherein the first and second thicknesses comprise an aggregate thickness and the first thickness constitutes less than or equal to about 75 percent of the aggregate thickness.

48. The method of claim 44, wherein the first thickness is less than about 550 Angstroms.

49. The method of claim 44, wherein the first thickness is between 450 Angstroms and 550 Angstroms.

50. The method of claim 44, wherein the forming of the second layer of polysilicon comprises forming the layer to have a sheet resistance which is greater than the sheet resistance of the first layer of polysilicon.

51. A method for enhancing data retention of a floating gate transistor comprising:

forming a floating gate over a substrate, the floating gate having an inner first portion and an outer second portion; and

providing conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion wherein forming a floating gate over a substrate comprises:

forming the inner first portion in contact with a gate dielectric; and

forming the outer second portion atop the inner first portion.

D3 cont.

52. The method of claim 51, wherein the forming of the floating gate comprises forming the inner first portion and the outer second portion to comprise polysilicon.

53. The method of claim 51, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise at least 25 percent of the floating gate thickness.

54. The method of claim 51, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise between about 25 to 75 percent of the floating gate thickness.

55. The method of claim 51, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration greater than or equal to 1×10^{18} cm^{-3}.

56. The method of claim 51, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration of greater than or equal to about 1×10^{18} cm^{-3}, with the outer second portion having a dopant concentration of less than 1×10^{18} cm^{-3}.

D3 cancel.

57. The method of claim 51, wherein:

the forming of the floating gate comprises forming a first layer of polysilicon over the substrate, the first layer defining the inner first portion, and after the forming of the first layer forming a second layer of polysilicon, the second layer defining the outer second portion.